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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,494	05/29/2007	Kozo Kimura	P30890	9808
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GREENBLUM & BERNSTEIN, P.L.C. 1950 ROLAND CLARKE PLACE RESTON, VA 20191				
EXAMINER TORRENTE, RICHARD T				
ART UNIT		PAPER NUMBER		
2482				
NOTIFICATION DATE		DELIVERY MODE		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/599,494

Applicant(s)

KIMURA ET AL.

Examiner

RICHARD TORRENTE

Art Unit

2482

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 September 0266 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/GS/US)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement "Texas Instruments ..." filed 1/9/07 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy and date of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because legal phraseology "comprises" is used. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim(s) 1-23 is/are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
6. Claim(s) 1, the phrase "the external device" renders the claim indefinite because the claim calls for 2 external devices. Thus, it is unclear which external device the claim "the external device" refers to.
7. Claim 6 recites the limitation "the timing of data". There is insufficient antecedent basis for this limitation in the claim.
8. Claim 17 recites the limitation "the control register". There is insufficient antecedent basis for this limitation in the claim.
9. Claim 20 recites the limitation "the in-field total" and "the inter-field difference". There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

10. Claim(s) 11 is/are objected to because of the following informalities: All abbreviations should be spelled out at the first occurrence. Appropriate correction is required. For the sake of prosecution, examiner will treat the abbreviations as general data.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-5, 9, 11, 12, 14 and 18-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Owen et al. (US 7,321,368).

Regarding claim 1, Owen discloses an integrated circuit for video/audio processing that processes video and audio signals (see abstract), comprising: a microcomputer block including a CPU (see 152 in fig. 3); a stream input/output block (see 186 in fig. 3) operable to receive/output video and audio streams (see 180 in fig. 3) to and from an external device (e.g. see 166 in fig. 3), under the control of said microcomputer block; a media processing block (see 80 in fig. 3) operable to execute media processing including at least one of compression and decompression (see 44, 46 and 180 in fig. 3) of the video and audio streams inputted to said stream input/output block or outputted from said stream input/output block under the control of said microcomputer block; an AV input/output block (see 200 in fig. 3) operable to convert the video and audio streams subjected to the media processing in said media processing block and output the video and audio streams to an external device (e.g. see

182 in fig. 3), or acquire the video and audio signals from the external device (e.g. see 164 in fig. 3) and convert the video and audio signals into video and audio streams to be subjected to the media processing in said media processing block, under the control of said microcomputer block (see 200, 190 and 80 in fig. 3); and a memory interface block operable (see 72 and 76 in fig. 3) to control data transfer between a memory (see 168 in fig. 3) and said microcomputer block, said stream input/output block, said media processing block and said AV input/output block, under the control of said microcomputer block (see interconnections in fig. 3).

Regarding claim 2, Owen further discloses wherein said microcomputer block, said stream input/output block, said media processing block and said AV input/output block are connected to said memory interface block by a dedicated data bus (e.g. see 167 in fig. 3), and the video and audio streams are exchanged through said memory among said microcomputer block, said stream input/output block, said media processing block and said AV input/output block (see 72 in fig. 3).

Regarding claim 3, Owen further discloses wherein said memory interface block is operable to relay the data transfer so that the data transfer between said memory and said microcomputer block, said stream input/output block, said media processing block and said AV input/output block is made in parallel (see 72 and 76 in fig. 3).

Regarding claim 4, Owen further discloses wherein said microcomputer block, said stream input/output block, said media processing block and said AV input/output block have no buffer memory for buffering the video and audio streams (see fig. 3).

Regarding claim 5, Owen further discloses wherein said microcomputer block, said stream input/output block, said media processing block and said AV input/output block store the video and audio streams in said memory and notify the other blocks of the storage (see 152, 72, 76 and 168 in fig. 3).

Regarding claim 9, Owen further discloses comprising: a signal line (see line between 72 and 82) which connects said stream input/output block and said media processing block, wherein said media processing block is operable to execute media processing of the video and audio streams inputted from said stream input/output block through said signal line or the video and audio streams to be outputted to said stream input/output block through said signal line (see 72 and 80 in fig. 3).

Regarding claims 11 and 18, Owen further discloses wherein said integrated circuit for video/audio processing is used as a system LSI (see 190 in fig. 3) for plural different devices; and the devices include a digital TV (see 182 in fig. 3), a digital video recorder, a video camera and a portable telephone.

Regarding claims 12 and 19, Owen further discloses wherein assuming that one of said devices is designated as a first device (see 166 in fig. 3) and another as a second device (see 164 in fig. 3) and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device (see 190 with 164 and 166 in fig. 3); in the case where the process is executed by said microcomputer block of said integrated circuit for video/audio processing for the first device, the process is executed by said microcomputer block of said integrated circuit for video/audio processing for the second device (see 152 in fig. 3); in the case where the process is executed by said stream input/output block of said integrated circuit for video/audio processing for the first device, the process is executed by said stream input/output block of said integrated circuit for video/audio processing for the second device (see 186 in fig. 3); in the case where the process is executed by said media processing block of said integrated circuit for video/audio processing for the first device, the process is executed by said media processing block of said integrated circuit for video/audio processing for the second device (see 80 in fig. 3); and in the case where the process is executed by said AV input/output block of said integrated circuit for video/audio processing for the first device, the process is executed by said AV input/output block of said integrated circuit for video/audio processing for the second device (see 200 in fig. 3).

Regarding claim 14, Owen further discloses wherein said media processing block has an instruction parallel processor which executes plural signal processing

instructions in parallel (see 52 to 44 and 46 in fig. 3); and in the case where one of the devices is designated as a first device and another as a second device, the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the instruction parallel processor of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other (see compatible mpeg coding/decoding in column 1, line 32).

Regarding claim 20, Owen further discloses wherein said AV input/output block is further operable to generate a recording video signal by converting the resolution (see 200 in fig. 3) of the video signal converted from the video stream subjected to media processing by said media processing block or acquired from an external device, as well as generating field feature information (see column 11, lines 47-51) indicating at least one of the in-field total (see column 3, lines 14-19) and the inter-field difference of the video fields indicated by the recording video signal (see column 9, lines 7-10); and said media processing block is further operable to access the field feature information and convert the recording video signal into a recording video stream (see 166 in fig. 3).

Regarding claim 21, Owen further discloses comprising a signal line (see interconnection between 200 and 80 in fig. 3) which connects said media processing block and said AV input/output block, wherein the field feature information is exchanged between said media processing block and said AV input/output block through said signal line (see column 11, lines 47-51 and 80 in fig. 3).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368).

Regarding claim 13, Owen discloses wherein in the case where one of the devices is designated as a first device and another as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate device), wherein the CPU of said integrated circuit for video/audio processing for the first device and the CPU of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible (e.g. H.261 in column 9, lines 32-34) with each other (see 80 in fig. 3).

Regarding claim 15, Owen further discloses wherein said media processing block has an instruction parallel processor which executes plural signal processing instructions in parallel (see 52 to 44 and 46 in fig. 3); and in the case where one of the devices is designated as a first device and another as a second device (see column 9,

lines 32-65, wherein it is implied that two user of fig. 3 will have separate CPU), the core of the CPU of said integrated circuit for video/audio processing for the first device and the core of the CPU of said integrated circuit for video/audio processing for the second device have the same logic connection (see fig. 3), and the core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have the same logic connection (see fig. 3).

Regarding claim 16, Owen further discloses wherein said media processing block has an instruction parallel processor which executes plural signal processing instructions in parallel (see 52 to 44 and 46 in fig. 3); and in the case where one of the devices is designated as a first device and another as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate CPU), the core of the CPU of said integrated circuit for video/audio processing for the first device and the core of the CPU of said integrated circuit for video/audio processing for the second device have the same mask layout (see fig. 3), and the core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have the same mask layout (see fig. 3).

Regarding claim 17, Owen further discloses wherein in the case where one of the devices is designated as a first device and another as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate CPU), the address of the control register for said stream input/output block, said media processing block, said AV input/output block and said memory interface block on the memory map of the CPU in said integrated circuit for video/audio processing for the first device is identical to the address of the control register for said stream input/output block, said media processing block, said AV input/output block and said memory interface block on the memory map of the CPU in said integrated circuit for video/audio processing for the second device (column 11, lines 28-44).

15. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368) in view of O'Sullivan (US 2005/0235134).

Regarding claims 6 and 7, Owen further discloses wherein said stream input/output block has an interface unit (see 186 in fig. 3) operable to transmit and receive the video and audio streams to and from said external device, an encryption processing unit (see 80 and 180 in fig. 3) operable to encrypt or decrypt the video and audio streams transmitted and received, and a direct memory access control unit (see 52 and 60 in fig. 2) operable to transfer data between said external device and said memory, said media processing block has an instruction parallel processor (see 52 to 44 and 46 in fig. 3) which executes plural signal processing instructions in parallel, and

a direct memory access control unit (see 52 in fig. 3) operable to control the data transfer with said memory, said AV input/output block has a graphics engine (see 200 in fig. 3) which executes graphics processing of image data, and a format conversion unit (see 200 in fig. 3) operable to convert the format of the video signal, and said memory interface block has plural ports (see 72 and 76 in fig. 3) connected to said microcomputer block, said stream input/output block, said media processing block and said AV input/output block, and has a memory scheduler (see 156, 154 and 82 in fig. 3) which adjusts the timing of data transfer at each of said plural ports.

Although Owen discloses decoding and encoding (see 80 in fig. 3) and control (see 156, 154 and 82 in fig. 3), it is noted that Owen does not disclose an accelerator which executes an arithmetic operation; wherein said microcomputer block further has at least one of a clock control unit operable to turn on/off the supply of a clock to said CPU and a power supply control unit operable to turn on/off the power supply.

However, O'Sullivan, in the same field of endeavor, discloses an optimizing processor wherein an accelerator (see ¶ [0083]) which executes an arithmetic operation; wherein said microcomputer block further has at least one of a clock control unit operable to turn on/off the supply of a clock to said CPU and a power supply control unit operable to turn on/off the power supply (see ¶ [0097]).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate O'Sullivan teachings of processor optimization into Owen parallel processor for the benefit of increasing processing efficiency and reducing power consumption.

Regarding claim 8, Owen, now incorporating the teaching of O'Sullivan, further discloses wherein said media processing block further has a data parallel processor which executes an arithmetic operation on plural pieces of data in parallel (see Owen 80 in fig. 3 and O'Sullivan ¶ [0083]).

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368) in view of Yamazaki (US 2004/0079952).

Regarding claim 10, although Owen discloses the blocks, it is noted that Owen does not disclose wherein circuit elements and wiring between the circuit elements in said microcomputer block, said stream input/output block, said media processing block, said AV input/output block and said memory interface block are formed on a circuit layer and a first wiring layer, respectively, on a semiconductor substrate; and said data bus is formed on a second wiring layer located above said first wiring layer.

However, Yamazaki, in the same field of endeavor, discloses a semiconductor fabrication wherein circuit elements and wiring between the circuit elements in said microcomputer block, said stream input/output block, said media processing block, said AV input/output block and said memory interface block are formed on a circuit layer and a first wiring layer, respectively, on a semiconductor substrate; and said data bus is

formed on a second wiring layer located above said first wiring layer (see 717, 719 and 720 in fig. 9D).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Yamazaki teachings of block layers into Owen blocks for the benefit of decreasing the bulk defect density and interface defect density formed in a crystalline semiconductor layer.

17. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368) in view of Smith (US 2005/0053028).

Regarding claim 22, Owen further discloses wherein said media processing block executes, a video data compressing or decompressing process (see 80 in fig. 3), and an audio data compressing or decompressing process for one video/audio multiplex stream (see 80 and 180 in fig. 3).

Although Owen discloses multiplexing or demultiplexing process (e.g. see 166 separated to 180 and 80 in fig. 3) for the stream, it is noted that Owen does not disclose a time division, a multiplexing or demultiplexing process for the stream, as well as prohibiting the multiplexing or demultiplexing process for the stream from being executed plural times within a predetermined time.

However, Smith, in the same field of endeavor, discloses a data protocol wherein a time division, a multiplexing or demultiplexing process for the stream (see ¶ [0004]),

as well as prohibiting the multiplexing or demultiplexing process for the stream from being executed plural times within a predetermined time (see ¶ [0023]).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Smith teachings of time division into Owen division for the benefit of a gateway and protocol which is capable of efficiently switching data between and among the circuit domain and the packet domain.

Regarding claim 23, Owen further discloses wherein said media processing block has a virtual multiprocessor functioning as plural logical processors (see 80, 158, 180, 200 in fig. 3) the compressing or decompressing process for said video data (see 80 in fig. 3), and the compressing or decompressing process for said audio data are executed by different logical processors (see 200 and 180 in fig. 3), respectively, which are the function of said virtual multiprocessor;

Although Owen discloses multiplexing or demultiplexing process (e.g. see 166 separated to 180 and 80 in fig. 3) for the stream, it is noted that Owen does not disclose a time division, a multiplexing or demultiplexing process for the stream, and the logical processor for executing the multiplexing or demultiplexing process for said stream sleeps until the expiry of the time on a predetermined timer after completion of the processing of a predetermined unit of said stream.

However, Smith, in the same field of endeavor, discloses a data protocol wherein a time division, a multiplexing or demultiplexing process for the stream (see ¶ [0004]), and the logical processor for executing the multiplexing or demultiplexing process for

said stream sleeps until the expiry of the time on a predetermined timer after completion of the processing of a predetermined unit of said stream (see ¶ [0023]).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Smith teachings of time division into Owen division for the benefit of a gateway and protocol which is capable of efficiently switching data between and among the circuit domain and the packet domain.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD TORRENTE whose telephone number is (571) 270-3702. The examiner can normally be reached on M-F: 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Young Lee/
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/Richard Torrente/
Examiner, Art Unit 2482